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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,136	09/22/2003	Kirt Reed Williams	10010900-1	2011

7590 02/16/2005

AGILENT TECHNOLOGIES, INC.
Intellectual Property Administration
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,136	WILLIAMS, KIRT REED	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09-22-03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1- 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski (US Pat. 5888884) in view of Greywall (US Pat. 6201631).

Regarding claims 1-9, Wojnarowski discloses a semiconductor structure (Fig. 8) comprising:

- a semiconductor core/die (70 in Fig. 8) having side surfaces (see left/right vertical surfaces in Fig. 8) including a first and a second side surface and a major/top surface , the semiconductor core/die material being a conventional silicon wafer/single crystal silicon (Col. 1-6)
- a layer of insulating material on the side surfaces (see 54 in Fig. 3-8), the insulating material including oxides of silicon such as SiO or SiO2 (Col. 7, lines 16-28)
- a plurality of interconnects/pads being positioned (see 40 in Fig. 8) over the major surface of the semiconductor core/die, the plurality of pads being on each

side surface including left/right side surfaces to provide the desired high density interconnect (HDI) structure (see Col. 6, lines 39-45)

- a plurality of electrically isolated and patterned electrodes/channels arrayed along the layer of the insulating material on the side surfaces including each left and right side surface (see one of the plurality of 62/64, shown as being connected with respective one of the plurality of interconnects/pads 40 on each side surface in Fig. 8; Col. 6, lines 37-43; Col. 7, lines 49-65; also see Col. 7, lines 63-65) and additionally arrayed over a major surface of the semiconductor core (see 62 on a top/horizontal surface connecting those on the side surfaces in Fig. 8), the major surface being orthogonal to said side surfaces
- the electrically isolated/patterned electrodes/channels including a conductive material such as aluminum, tungsten, etc. (Col. 7, line 44)
- the isolated/patterned electrodes extending substantially in a direction orthogonal to the major surface (see 62 on the side surfaces in Fig. 8) of the semiconductor core, and
- the plurality of interconnects/pads being positioned over the major surface of the semiconductor core/die and being electrically connected to respective/selected electrically isolated/patterned electrodes to achieve the desired power, ground or other/input-output (I/O) connections (Fig. 8; Col. 7, lines 45-65)

(Fig. 8; Col. 6, line 20- Col. 8, line 20).

Wojnarowski fails to teach the conductive material having etch selectivity with respect to the insulating material.

Greywall teaches using conventional deep reactive ion etch system (DRIE) to etch silicon/polysilicon/silicon oxide structure where an etchant having etch selectivity with respect to the oxide/insulating material (Fig. 4 and 5; Col. 5, lines 30-65). Greywall further teaches using a conventional conductive electrode material including a silicon based material such as doped polysilicon or aluminum (Col. 6, lines 35-45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive material having etch selectivity with respect to the insulating material as taught by Greywall so that the electrode profile can be improved and undercut can be prevented in Wojnarowski's structure.

Regarding claims 10-15, Wojnarowski and Greywall teach substantially the entire structure as applied to claims 1-9 above.

Response to Arguments

3. Applicant's arguments filed on 11-30-04 have been fully considered but they are not persuasive.

A. Applicant contends that there is no motivation to combine Greywall with Wojnarowski to provide the conductive material having etch selectivity.

However, as explained above, Wojnarowski fails to teach the conductive material having etch selectivity with respect to the insulating material. Greywall teaches using conventional deep reactive ion etch system (DRIE) to etch the conductive material such as polysilicon where an etchant has etch selectivity with respect to the oxide/insulating material (Fig. 4 and 5; Col. 5, lines 30-65; Col. 6, lines 35-45). Such conductive structure and etch process provides an improved metal removal/etch and profile, reduced undercut and improved HDI reliability. Therefore, Greywall is combined Wojnarowski to provide the desired improvements in Wojnarowski's HDI/metallization structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

02-10-05

NITIN PAREKH

PATENT EXAMINER

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